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09/359,056	07/21/1999	BARMAK MANSOORIAN	08305/038001	2286

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	21

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/359,056	MANSOORIAN, BARMAK	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004 and 07 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15 and 16* is/are rejected.

7)☒ Claim(s) *14 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 1/7/2004 with respect to claims 1-17 have been considered but are moot in view of the new ground of rejection. In addition to the new ground of rejection, the Examiner would like to address the Applicant's arguments regarding the teaching of Pain and Pickering and a newly added limitation of an active impedance matching device.

The Applicant argues that Pain and Pickering do not disclose any suggestion or motivation to modify Pain with Pickering (page 6). However, as motivated by Pickering described in **col. 2, lines 17-26**, the off-chip data is transmitted as differential signal to minimize the effects of common-mode noise and matching of the transmission line (implying impedance matching) is performed to minimize problems of noise caused by reflections. Therefore, the combination of Pain and Pickering has been established at least based on the motivation to minimize noises.

The Applicant further requests the Examiner to provide documentary evidence to support the conclusion that a variable resistor can be implemented using a transistor with adjustable bias current (page 8). The Examiner respectfully submits a reference to Saari (US 4,441,080) to support the teaching of variable resistance by changing the bias current of a transistor (see Saari, col. 2, lines 54-58).

Furthermore, in response to the Applicant's arguments for an **active** impedance matching device not being taught by Pain and Pickering (page 6), the Examiner respectfully submits that

an active impedance matching device is met by the combination of Pain and Pickering in view of Gabara (US 5,739,714) for matching variable impedance implemented with transistors which act as an active termination circuit to match the impedance of transmitter's output to the impedance of receiver's input. It is noted that transistors are active elements while resistors are passive elements as fully supported by Gabara in col. 4, lines 35-41.

Additionally, because the Applicant has not traversed the Examiner's assertion of Official Notice of claim 12, the lack of traversal is an admission that the current source in Pickering may be considered as a current mirror is admitted as being prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Pickering et al (US 5,050,194) and in further view of Gabara (US 5,739,714).

Regarding claim 1, Pain discloses an image sensor, comprising:

an image acquisition portion (100, 112) as shown in figs. 1A-1C, col. 3, lines 52-63;

an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current mode output (see fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output. Since the ADC array is configured with CMOS current driving mode, the impedance must exist at the ADC array output and throughout transmission line(s).

Pain's disclosure of digital output 110 (figs. 1A-1C) suggests another separate portion (i.e., another chip) to be connected thereto for receiving digital image data output from the ADC array. The suggested separate portion represents "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs...and said image receiving portion receiving current mode output" in order to form a complete imaging system of CMOS compatible applications (see col. 2, lines 5-7 for a consistent CMOS compatible).

Therefore, it would have been obvious to one of ordinary skill in the art to recognize another chip connected to the digital output from the image processing portion (ADC array 118) as an image receiving portion which would be also configured in CMOS having input characteristics being compatible with the digital output of the image processing portion to function in a complete imaging system.

Pain does not explicitly disclose the CMOS outputs being differential outputs and an active impedance matching device being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion.

As taught by Pickering, differential output driver (1) and differential input driver (8) are implemented in CMOS technology for transmitting and receiving off-chip data, and matching impedances of the drivers with transmission line is also performed at the output and input of the drivers to minimize common mode noise and noise caused by reflections (see Fig. 1; col. 2, lines 17-26, 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art to combine Pain with the teaching of Pickering for differential output and input drivers of the devices using CMOS technology with a corresponding impedance matching device to transmit and receive off-chip data thereby common mode noise and noise caused by reflections would be minimized.

Although Pickering teaches the CMOS differential output and input drivers and the corresponding **passive** impedance matching device using a passive termination circuit (resistors), Pickering fails to teach an **active** impedance matching device. However, the active impedance matching device using an active termination circuit implemented with transistors is an obvious variant over the passive one in circuit design for variably controlling impedance as taught by Gabara in col. 4, lines 35-41.

Therefore, it would have been obvious to one of ordinary skill in the art to implement the impedance matching device using active impedance elements such as transistors to variably control (variable load) the impedance of the devices in the combination of Pain and Pickering as an obvious circuit design variation over the passive one.

Regarding claim 2, the image processing portion includes a portion with a CMOS output (3) as shown by Pickering in Fig. 1.

Regarding claims 3 & 6, Pickering also discloses that impedance matching circuits (termination circuits 6) are implemented at both ends (see Fig. 1; col. 2, lines 59-61). It is noted that the analysis in claim 1 for active termination circuit is also applied in these claims.

Regarding claim 4, Pickering discloses a current source (shown in block 3 of Fig. 1) used to bias the transistors wherein the corresponding impedance inherently exists at the output of each transistor in response to the bias current.

Regarding claim 5, the output impedance is matched to input impedance of the image receiving circuit as analyzed in claim 1.

Regarding claim 7, Pickering shows differential input buffer (8) at the receiver (7). It is noted that the same analysis in claim 4 is applied to claim 7 for the input impedance.

Regarding claim 8, the input impedance is matched to output impedance of the image receiving circuit as analyzed in claim 1.

Regarding claim 9, the claimed limitations are analyzed with respect to claims 3 & 6.

Regarding claim 10, the claimed limitations are analyzed with respect to claims 4 & 7.

Regarding claim 11, the claimed limitations are analyzed with respect to claims 5 & 8.

Regarding claim 12, Pickering shows a current source used for biasing the transistors in the differential buffer 3 (Fig. 1). Pickering does not teach that the current source is a current mirror part. However, an Official Notice is taken that the current source can be configured by current mirror in CMOS applications.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize an alternative configuration for the current source in Pickering would be a well known current mirror.

Regarding claim 13, Pain discloses the image acquisition circuit being an active pixel sensor (APS 300) with a photosensor (photogate 310), an in-pixel buffer (floating diffusion 330, transistor 360), and in-pixel select transistor (vertical select 370) (see fig. 3A; col. 6, lines 25-49).

Regarding claim 15, Pain, Pickering and Gabara disclose all limitations of claim 15 except for explicitly disclosing the limitation of matching impedances by adjusting bias current through at least one biased device in a way that renders the input impedance relatively independent of an input current. Pickering and Gabara teach passive or active termination circuit connected at both transmitter and receiver ends to match impedances as analyzed in claim 1. An Official Notice is further taken that the active impedance transistors can provide variable termination resistance (variable load) by changing bias current of the transistors.

Therefore, it would have been obvious to one of ordinary skill in the art to adjust bias current of the active impedance transistors so that variable impedance control between the transmitter and the receiver would be realized independent of an input current.

Regarding claim 16, the claimed limitations are analyzed with respect to claim 1.

Allowable Subject Matter

4. Claims 14 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fails to teach or suggest that the image acquisition portion and the image processing portion operates at substantially zero voltage.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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